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Hironaka et al.

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(54) **MULTI-PORT INTEGRATED CACHE**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 512 days.

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(57) **ABSTRACT**

(51) **Int. Cl.**

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A multi-port instruction/data integrated cache which is provided between a parallel processor and a main memory and stores therein a part of instructions and data stored in the main memory has a plurality of banks, and a plurality of ports including an instruction port unit consisting of at least one instruction port used to access an instruction from the parallel processor and a data port unit consisting of at least one data port used to access data from the parallel processor. Further, a data width which can be specified to the bank from the instruction port is set larger than a data width which can be specified to the bank from the data port.

(52) **U.S. Cl.** **711/131; 711/123; 711/149**

(58) **Field of Classification Search** None
See application file for complete search history.

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5 Claims, 25 Drawing Sheets

