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Hironaka et al.

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(54) **MULTI-PORT INTEGRATED CACHE**

6,029,242 A * 2/2000 Sidman 712/42
6,378,050 B1 4/2002 Tsuruta
6,647,465 B2 11/2003 Kametani

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(Continued)

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FOREIGN PATENT DOCUMENTS

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JP 4-257949 A 9/1992
JP 2002-55879 A 2/2002

OTHER PUBLICATIONS

(21) Appl. No.: **12/034,454**

Mattausch, H.J., "Hierarchical Architecture for Area-Efficient Integrated N-Port Memories With Latency-Free Multi-Gigabit Per Second Access Bandwidth," Electronics Letters 35(17):1441-1443, 1999.

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(30) **Foreign Application Priority Data**

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(57) **ABSTRACT**

(51) **Int. Cl.**
G06F 12/00 (2006.01)

A multi-port instruction/data integrated cache which is provided between a parallel processor and a main memory and stores therein a part of instructions and data stored in the main memory has a plurality of banks, and a plurality of ports including an instruction port unit consisting of at least one instruction port used to access an instruction from the parallel processor and a data port unit consisting of at least one data port used to access data from the parallel processor. Further, a data width which can be specified to the bank from the instruction port is set larger than a data width which can be specified to the bank from the data port.

(52) **U.S. Cl.** **711/131**; 711/123; 711/149; 365/230.05

(58) **Field of Classification Search** 711/3, 711/5, 123, 131, 149, 170; 365/230.05
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,784,630 A 7/1998 Saito

11 Claims, 25 Drawing Sheets

